Priyank Faldu

PhD Student, The University of Edinburgh

Research Interests

Broad: Computer system research and the interaction between software and hardware
Current Focus: Cache and memory subsystems

Education

Doctor of Philosophy, *Oct 2014 – Present*[*]
School of Informatics, The University of Edinburgh, United Kingdom
Thesis: Efficient Cache Management Techniques for Traditional and Emerging Workloads
Advisor: Dr. Boris Grot

Master of Technology, *Jul 2008 – Jun 2010* CGPA : 10.00/10.00
Computer Science and Engineering, Indian Institute of Technology Kanpur (IITK), India
Thesis: CUDA-LF: A Lock-Free Data Structure Library for GPGPU
Advisor: Prof. Mainak Chaudhuri

Bachelor of Technology, *Jul 2004 – May 2008* CGPA : 8.39/10.00
Computer Engineering, Institute of Technology, Nirma University, Ahmedabad, India

Publications

P. Faldu, J. Diamond, B. Grot. A Closer Look at Lightweight Graph Reordering. *In Proceedings of the International Symposium on Workload Characterization [IISWC], Nov 2019.*

P. Faldu, J. Diamond, B. Grot. POSTER: Domain-Specialized Cache Management for Graph Analytics. *In Proceedings of the 28th International Conference on Parallel Architectures and Compilation Techniques [PACT], Sep 2019.*

P. Faldu, B. Grot. Leeway: Addressing Variability in Dead-Block Prediction for Last-Level Caches. *In Proceedings of the 26th International Conference on Parallel Architectures and Compilation Techniques [PACT], Sep 2017.*

P. Faldu, B. Grot. Reuse-Aware Management for Last-Level Caches. *In 2nd International Cache Replacement Championship Workshop [CRC], co-located with ISCA, Jun 2017.*

P. Faldu, B. Grot. LLC Dead Block Prediction Considered Not Useful. *In 13th International Workshop on Duplicating, Deconstructing and Debunking [WDDD], co-located with ISCA, Jun 2016.*

Patents

P. Faldu, J. Diamond, A. Patel. Cache Memory Architecture and Policies for Accelerating Graph Algorithms. *ID: US20180129613A1, Assignee: Oracle International Corporation, Publication: May 10, 2018.*

J. Koh, A. Oberoi, G. P. Sharma, R. Velappan, **P. Faldu**. Parallelization Method and Electronic Device Based on Profiling Information. *ID: US20160004570A1, Assignee: Samsung Electronics Co., Ltd., Publication: Jan 7, 2016.*

Grant

Oracle ERO Award: Efficient Scale-Up Graph Processing on Future Memory Systems.
Co-authored the grant proposal; PI: Boris Grot; Award: $76,000; Year: 2017.

Professional Activities

Organizing Committee : Web Co-chair, International Symposium on Computer Architecture (ISCA), 2018
Peer-Reviews: Computer Architecture Letters (CAL)

Research Internships

Research Assistant, Oracle Labs, Austin, USA, *May 2016 – Sep 2016*

Project	:	Improving Cache Efficiency for Graph Analytics Applications
Team Size	:	3
Description	:	Demonstrated that underutilization of on-chip caches leads to poor performance of graph analytics applications and proposed a software-hardware co-design to improve the cache efficiency for graph-analytic applications. A patent application has been filed for the resultant design.

Professional Experience [4 years]

Lead Engineer, Samsung R&D Institute India, *Jul 2013 – Aug 2014*

As a senior member of the Android Graphics team, I was responsible for exploring the applicability of OpenCL in multimedia related applications for the company's flagship Galaxy devices.

Project	:	Accelerating HDR and Bokeh Image Processing Algorithms for Smart Camera
Technologies	:	OpenCL
Team Size	:	5
Description	:	Successfully accelerated the multimedia applications using GPUs and achieved 10%–30% speed-up over the highly optimized CPU code in same or lower power budget for ARM Mali & Qualcomm Adreno GPU. Additionally, accelerated PNG encoder and decoder implementation by devising parallel algorithms.

Graphics Hardware Engineer, Intel Technology India Pvt. Ltd., *May 2011 – Jul 2013*

Part of a path-finding team responsible for proposing new features and analyzing feasibility of proposed features for future generation integrated-GPU architectures and development of various tools to assist in the study.

Project	:	Functional Simulator of Multi-Threaded Execution Unit of GPU
Technologies	:	C++, Boost Parser Framework
Team Size	:	1
Description	:	Developed functional simulator to implement GPU's Instruction Set Architecture along with associated features like SIMD execution, control-flow management, barrier synchronization, register-file management, memory management, instruction predication and other Intel specific features. Have contributed in all the phases of the project covering proposal, design, development and validation.

Project	:	Functional Simulator for OpenCL Applications
Role	:	Characterizing OpenCL workloads & Maintenance of the tool
Technologies	:	C++, LLVM open-source interpreter, Instrumentation Library for Statistical Profiling
Team Size	:	3
Description	:	Contributed to the development of a functional simulator for OpenCL applications. Carried out workload characterization studies for many OpenCL benchmarks using this simulator.

Project	:	Performance Debug on Silicon
Technologies	:	Performance Profiler
Team Size	:	1
Description	:	Carried out debug for performance issue on an OpenCL application, benchmarking the global memory bandwidth on a next generation GPU. After the analysis of assembly code and with the help of performance profiler, I successfully tracked down the issue and devised a solution.

Additional Responsibilities
- Mentored two M.Tech. interns for a period of 10 months.
- Interviewed candidates for the post of full-time senior engineer to assess their software and problem-solving skills.
- Represented my team in the campus-hire programme at Nirma University, Ahmedabad to recruit interns.

Software Engineer, Google India Pvt. Ltd., *Jul 2010 – Mar 2011*

Product	:	Google Map Maker
Technologies	:	C++, JavaScript and Google technologies like Map-Reduce, Protocol-Buffers etc.
Team Size	:	20+
Description	:	Developed various UI features and a module to analyze user-engagement for the Google Map Maker product.

Academic Achievements

- Received *Academic Excellence Award* at IIT Kanpur for the year 2008–09
- Topper of the M. Tech. batch 2008–10, IIT Kanpur
- All India Rank 263 in *Graduate Aptitude Test in Engineering (GATE)* 2008
- Among Top 8% students in All India *Common Admission Test (CAT)* 2007
- Topper of the 10^{th} grade batch 2001–02 and Ranked 15^{th} in Rajkot City

Academic & Mentoring Activities

- Mentored two students for their *B. Tech. Honors Project* and one student for his *Research Internship* at The University of Edinburgh
- Tutoring at The University of Edinburgh for the courses of *Computer Architecture* and *Introduction to Computer Systems*
- Teaching Assistant at The University of Edinburgh for the course of *Parallel Architectures*, *Operating Systems*, and *Introduction to Computer Systems*
- Tutoring at IIT Kanpur for the course of *Fundamentals of Computing*
- Teaching Assistant at IIT Kanpur for the courses of *Fundamentals of Computing* and *Operating Systems*

Internships/Workshops

- Interned at *Tata Consultancy Services (TCS), Gandhinagar*, Jan–Apr 2008
- Attended 11^{th} International Summer School on *Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems* (ACACES) held by HiPEAC, Jul 12–18, 2015
- Attended *IBM Research - India Collaborative Academia Research Exchange* (I-CARE) workshop, Oct 26, 2009
- Demonstrated a student project in the workshop on *Program Optimization for Multi-Core Architecture* held at IIT Kanpur, Jun 29–Jul 4, 2009
- Attended workshop on *Optimizing Performance of Parallel Programs on Emerging Multi-Core Processors and GPUs* jointly organized by CDAC, Pune and IIT Madras, Jun 1–5, 2009
- Attended *Infosys Campus Connect* summer programme held at Nirma University, Ahmedabad, May–Jun 2007