Priyank Faldu

RESEARCH INTERESTS

Computer Architecture, Parallel Computing

EDUCATION

Doctor of Philosophy October, 2014 - Present*
School of Informatics, University of Edinburgh, United Kingdom
Thesis: Efficient Cache Management Strategies for Traditional and Emerging Workloads
Advisor: Dr. Boris Grot

Master of Technology July, 2008 - June, 2010 **CGPA : 10.00/10.00**
Department of Computer Science and Engineering, Indian Institute of Technology Kanpur

Bachelor of Technology July, 2004 - May, 2008 **CGPA : 8.39/10.00**
Department of Computer Engineering, Institute of Technology, Nirma University, Ahmedabad

PROFESSIONAL EXPERIENCE [~4 years]

Lead Engineer, **Samsung R&D Institute India** July, 2013 - August, 2014
As a senior member of the Android Graphics team, responsible for exploring the applicability of OpenCL in multimedia related applications for the company's flagship Galaxy devices. Have successfully accelerated two multimedia applications using GPUs and achieved 10%-30% speed-up over the highly optimized CPU code in same or lower power budget.

Graphics Hardware Engineer, **Intel Technology India Pvt. Ltd.** May, 2011 - July, 2013
Part of a team responsible for proposing new features and analyzing feasibility of proposed features for future generation integrated-GPU architectures and development of various tools to assist in the study.

Functional Simulator of Multi-Threaded Execution Unit of GPU
Technologies : C++, Boost Parser Framework
Role : Development and Validation of the tool, Shader level analysis
Team Size : 1
Developed functional simulator to implement GPU's Instruction Set Architecture along with associated features like SIMD execution, control-flow management, barrier synchronization, register-file management, memory management, instruction predication and other Intel specific features. Have contributed in all the phases of the project covering proposal, design, development and validation.

Functional Simulator for OpenCL Applications
Technologies : C++, LLVM open-source interpreter, Instrumentation Library for Statistical Profiling
Role : Characterizing OpenCL workloads & Maintenance of the tool
Team Size : 3
Contributed to the development of functional simulator for OpenCL applications. Carried out workload characterization studies for many OpenCL benchmarks using this simulator.

Performance Debug on Silicon
Technologies : Performance Profiler
Team Size : 1
Carried out debug for performance issue on an OpenCL application, benchmarking the global memory bandwidth on a next generation GPU. After the analysis of assembly code and with the help of performance profiler, I successfully tracked down the issue and devised a solution.

Additional Responsibilities
- Mentored two M.Tech. interns for a period of 10 months
- Interviewed candidates for the post of full-time senior engineer to assess their software and problem-solving skills
- Represented my team in the campus-hire programme at Nirma University, Ahmedabad to recruit interns

Software Engineer, **Google India Pvt. Ltd.** July, 2010 - March, 2011
Google Map Maker
Technologies : C++, JavaScript and Google technologies like Map-Reduce, Protocol-Buffers etc.
Team Size : 20+
Developed UI features and a module for user-engagement analysis for the Google Map Maker.

PUBLICATIONS

- **Leeway: Addressing Variability in Dead-Block Prediction for Last-Level Caches** [PACT'17]
  Priyank Faldu and Boris Grot
  In Proceedings of the 26th International Conference on Parallel Architectures and Compilation Techniques, September 2017
- **Reuse-Aware Management for Last-Level Caches** [CRC'17]
  Priyank Faldu and Boris Grot
  In 2nd International Cache Replacement Championship Workshop, co-located with ISCA, June 2017
- **LLC Dead Block Prediction Considered Not Useful** [WDDD'16]
  Priyank Faldu and Boris Grot
  In 13th International Workshop on Duplicating, Deconstructing and Debunking, co-located with ISCA, June 2016

PATENTS

- **Parallelization Method and Electronic Device**
  Jaehan Koh, Anuradha Oberoi, Gopalakrishna Puligedda Sharma, Raghavan Velappan and Priyank Faldu
  U.S. Patent: 20160004570, Assignee: Samsung Electronics Co., Ltd., Issuesd: January 7, 2016

MASTER'S THESIS

CUDA-LF: A Lock-Free Data Structure Library for GPGPU
Advisor : Dr. Mainak Chaudhuri & Prof. Sanjeev K. Aggarwal
Technologies : C++, CUDA Framework on Nvidia® Tesla® GPU
Designed a lock-free library for concurrent linked-list operations and concurrent breadth-first-search on graphs for GPUs. Also devised a lock-free scalable concurrent algorithm to perform breadth-first-search on large graphs. These GPU implementations achieved speed-up of up to 300%-600% over their CPU implementations.

ACADEMIC PROJECTS

- **Implementation of BGE on SMP architecture**
- C, OpenMP library, GNU Multiple-Precision library
- Implemented a '*Bidirectional Gaussian Elimination*' for dense matrices of order 10^4 over GF(P), Galois Field over prime number P, on Shared Memory Multi-Processors as a part of the course Parallel Semi-Numerical and Non-Numerical Algorithms and achieved a speed-up of up to 952% on a 16-core machine.
- **Implementation of a library of Concurrent Data Structures**
- C++, PThread library
- Implemented '*Concurrent Lock-Free Data Structures*' such as linked-list, queue, skip-list, heap, hash-table etc. as part of the project of the course Concurrent Data Structures. All implementations were profiled on a 16-core machine.
- **Implementation of the LRPD run-time Library**
- C, OpenMP library
- Implemented a simulation of a run-time library for '*Lazy Reduction and Privatization test for DOALL*' as a part of the course Advanced Compiler Optimizations and achieved a speed-up of up to 385% on a 4-core machine.
- **Feasibility study of EMD in character matching in scanned documents**
- C, Matlab (for preprocessing of documents)
- Studied an application of '*Earth Mover's Distance*' in matching images of handwritten characters as a part of the course Indexing and Searching Techniques in Databases.

ACADEMIC ACHIEVEMENTS

- Completed the MOOC on *Heterogeneous Parallel Programming* by Professor Wen-Mei Hwu of the University of Illinois at Urbana-Champaign in February 2013 communication in December 2013
- Received *Academic Excellence Award* at IIT Kanpur for the year 2008-09
- Topper of the M.Tech. batch 2008-10, IIT Kanpur
- All India Rank 440 and 263 in *Graduate Aptitude Test in Engineering* 2007 and 2008 respectively
- Among Top 8% students in All India *Common Admission Test* 2007
- Topper of the 10th grade batch 2001-02 and Ranked 15th in Rajkot City

INTERNSHIPS/WORKSHOPS

- Interned at '*Oracle Labs, Austin*' from May to September 2016'
- Interned at '*Tata Consultancy Services, Gandhinagar*' from January to April 2008
- Attended 11th International Summer School on '*Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems*' (ACACES) held by HiPEAC from July 12 to 18, 2015
- Attended 47th International Symposium on '*Microarchitecture*' held from December 13 to 16, 2014
- Attended 16th International Symposium on '*High-Performance Computer Architecture*' held from January 9 to 14, 2010
- Attended '*IBM Research - India Collaborative Academia Research Exchange*' (I-CARE) workshop held on October 26, 2009
- Demonstrated a student project in the workshop on '*Program Optimization for Multi-Core Architecture*' held at IIT Kanpur during June 29 to July 4, 2009
- Attended tech-workshop on '*Optimizing Performance of Parallel Programs on Emerging Multi-Core Processors and GPUs*' from June 1 to 5, 2009 jointly organized by CDAC, Pune and IIT Madras
- '*Infosys Campus Connect*' programme held at Nirma University, Ahmedabad from May 2007 to June 2007

ACADEMIC & PROFESSIONAL ACTIVITIES

- Web co-chair of the 45th '*International Symposium on Computer Architecture (ISCA)*' 2018
- Tutor for the courses of '*Introduction to Computer Systems*' and '*Computer Architecture*' at University of Edinburgh
- Teaching Assistant for the course of '*Parallel Architectures*' at University of Edinburgh
- Tutor for the course of '*Fundamentals of Computing*' at IIT Kanpur
- Teaching Assistant for the courses of '*Fundamentals of Computing*' and '*Operating Systems*' at IIT Kanpur
- Team Member of the '*Departmental Post-Graduate Placement Committee*' at IIT Kanpur from June to December, 2009

PROGRAMMING TECHNOLOGIES

- Proficient in C, C++, OpenCL
- Working knowledge of CUDA Programming Language, PThread, OpenMP
- Familiar with Python, Perl, Shell Scripting, Core Java